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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,616	03/09/2001	Yatin V. Hoskote	2207/10554	7643

7590 07/08/2004

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,616	HOSKOTE ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been presented for examination based on applicant's disclosure filed on 9 March 2001. Claims 1-21 have been rejected by the examiner.

Drawings

2. The drawings filed 9 March 2001 have been reviewed and approved by the examiner pending review by the draftsperson.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,247,163 issued to Burch et al.

Independent claims 1, 18, and 20 are drawn to:
Method for mapping state elements between first and second circuit by:
Comparing state element features (structural phase) in first circuit to second
Determining mappings between state elements in first and second circuit
Accounting for "don't care" conditions before comparing before comparing
Detecting polarity (inversion detection) of mappings
Comparing state element (functional phase) equivalence by three-valued simulation
Determining further mappings from functional phase
Detecting threshold condition for completion

Regarding independent claims 1, 18, and 20: Burch discloses the elements of the claimed limitations of the present invention as follows:

- Method for mapping state elements between first and second circuit: Burch discloses the mapping of state (latch) elements between a first and second circuit (Abstract, Summary of Invention, CL12-L14, 44, Figs. 5-8B)

- Comparing state element features (structural phase) in first circuit to second: Burch discloses comparing (determining correspondence) between a first and second circuit (CL9-L17-CL10-L33, CL11-L3-10, 29-35, Figs. 5-8B). The examiner has interpreted this process to be functionally equivalent to the structural phase of the claimed invention that compares element features between a first and second circuit.

- Determining mappings between state elements in first and second circuit: Burch discloses determining mappings between state elements of a first and second circuit (CL7-L38, CL11-L35-38, Figs. 5-8B).

- Accounting for "don't care" conditions before comparing before comparing: Burch considers don't care conditions in mapping state elements (Abstract, CL2-L53, CL9-L17, Figs. 5-8B).

- Detecting polarity (inversion detection) of mappings: Burch discloses inversion detection of combined state element mappings (CL3-L33-CL5-L5).

- Comparing state element (functional phase) equivalence by three-valued simulation: Burch considers equivalence of three state values (CL12-L14, 44).

- Determining further mappings from functional phase: Burch performs further mapping after considering equivalence (CL9-L17-CL10-L33, CL11-L39-44).

- *Detecting threshold condition for completion: Burch discloses a completion condition (Fig. 8B, 870).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,247,163 issued to Burch et al in view of U.S. Patent 6,651,225 issued to Lin et al.

Regarding independent claims 1, 18, and 20: As cited previously, Burch discloses the elements of the claimed limitations of the present invention as follows:

- Method for mapping state elements between first and second circuit: Burch discloses the mapping of state (latch) elements between a first and second circuit (Abstract, Summary of Invention, CL12-L14, 44, Figs. 5-8B).

- Comparing state element features (structural phase) in first circuit to second: Burch discloses comparing (determining correspondence) between a first and second circuit (CL9-L17-CL10-L33, CL11-L3-10, 29-35, Figs. 5-8B). The examiner has interpreted this process to be functionally equivalent to the structural phase of the claimed invention that compares element features between a first and second circuit.

- Determining mappings between state elements in first and second circuit: Burch discloses determining mappings between state elements of a first and second circuit (CL7-L38, CL11-L35-38, Figs. 5-8B).

- Accounting for "don't care" conditions before comparing before comparing: Burch considers don't care conditions in mapping state elements (Abstract, CL2-L53, CL9-L17, Figs. 5-8B).

- Detecting polarity (inversion detection) of mappings: Burch discloses inversion detection of combined state element mappings (CL3-L33-CL5-L5).

- Comparing state element (functional phase) equivalence by three-valued simulation: Burch considers equivalence of three state values (CL12-L14, 44).

- Determining further mappings from functional phase: Burch performs further mapping after considering equivalence (CL9-L17-CL10-L33, CL11-L39-44).

- Detecting threshold condition for completion: Burch discloses a completion condition (Fig. 8B, 870).

Burch does not explicitly disclose elements relating to determining equivalence between circuits based on fan-in and fan-out (equivalence) in mapping state elements as recited in the limitations of dependent claims 2-17.

Per dependent claims 2-17, 19, and 21: Lin discloses determining fan-in and fan-out sets of combinational components (elements) that the examiner has equated to be functionally equivalent to the fan-in and fan-out signatures of the claimed invention. (Lin: CL58-L39-CL60-L13, Fig. 16) The limitations relating to parallel comparisons (claims 10, 11) are inherently disclosed by Burch since the equivalence comparisons cited above are performed between two circuits simultaneously. (Burch: CL9-L17-CL10-L33, CL11-L3-10, 29-35, Figs. 5-8B) Burch also discloses inputting random values during equivalence comparisons as recited in the limitations of claims 6, 13, 14, 19, and 21. (Burch: Abstract, Summary of Invention, Fig. 3A)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings Burch relating to determining mappings between state elements of a first and second circuit, with the teachings of Lin relating to determining fan-in and fan-out sets of combinational components (elements), to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with

many types of equivalence verification process available for VLSI circuit development in the market place and large amounts of money being spent in product development and improvement. (see U.S. 6,496,955 Background for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Burch with the teachings of Lin in order to reduce development time and cost.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,496,955 issued to Chandra et al discloses mapping of component elements in equivalence verification.

U.S. Patent 6,035,109 issued to Ashar et al discloses mapping of component elementś in equivalence verification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

Application/Control Number: 09/802,616

The Official Fax Numbers are:

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